High Speed Receiver Circuitry for Operation in the Sub-THz Wave Band

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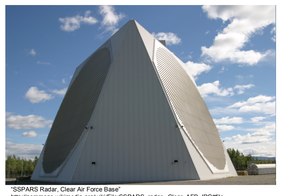
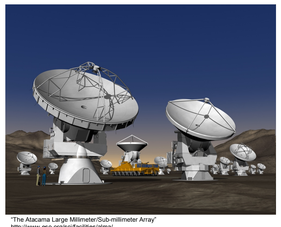
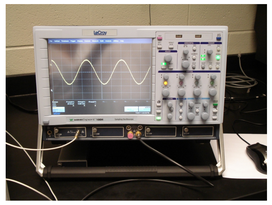
MOTIVATION



"SSPARS Radar, Clear Air Force Base"
http://commons.wikimedia.org/wiki/File:SSPARS_radar,_Clear_AFB.JPG#file



"The Atacama Large Millimeter/Sub-millimeter Array"
http://www.eso.org/sci/facilities/alma/

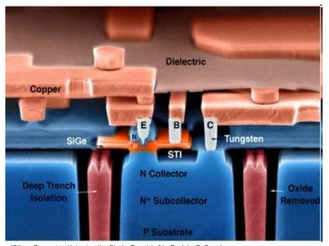


Applications in:

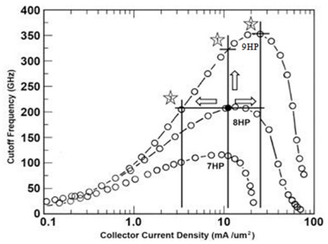
- •Communications
- •Radar
- •High Speed Sampling Oscilloscopes
- •Software Defined Radio
- •Digital Signal Processing

APPROACH

- •Designed using Cadence Design Systems' software suite
- •Utilized Technology kits form IBM and Houghes Research Labs.
- •The kit employed from IBM in this work is 8HP, a SiGe BiCMOS process, from which we have made use of its high f_T HBT's.
- •Houghes Research Labs' G4, an INP kit also used that boasts HBT's with an even higher f_T of 0.35THz and an f_{max} of 0.4THz. One of the receivers produced in the IBM SiGe kit has been reproduced in this InP kit to improve performance.
- •Using a combination of advanced kits and novel circuit design techniques these receiver designs were made possible.



"Silicon-Germanium Heterojunction Bipolar Transistor" by Dr. John D. Cressler,
http://users.ece.gatech.edu/~cressler/



PREVIOUS WORK

D. Cui, D. Sawdaii, S. Hsu, D. Pavlidis, "Low DC Power, High Gain-Bandwidth Product, Coplanar Darlington Feedback AMPL-RS Using InALAs/InGaAs Heterojunction Bipolar Transistors," GaAs IC Symp. 2000, pp259-262

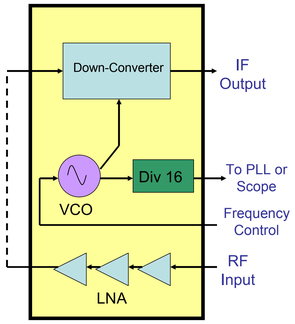
O. Wohlgemuth, P. Paschke, and Y. Baeyens, "SiGe broadband amplifiers with up to 80 GHz bandwidth for optical applications at 43 Gbit/s and beyond," in Proc. IEEE 33rd Eur. Microwave Conf., Oct. 2003, pp. 1087–1090.

W. Perndl, W. Wilhelm, H. Knapp, M. Wurzer, K. Aufinger, T. F. Meister, J. Bock , W. Simburger, A. L. Scholtz, "A 60 GHz Broadband Amplifier in SiGe Bipolar Technology," in IEEE BCTM

J. Kim, J. F. Buckwalter, "A DC-102GHz Broadband Amplifier in 0.12um SiGe BICMOS," in RFIC Symposium, June 2009, pp. 53-56

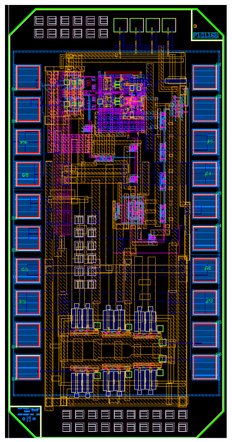
B. Agarwal et al., "112-GHz, 157-GHz, and 180-GHz InP HEMT Traveling-wave Amplifiers," IEEE Trans. Micro. Theory and Techniques, vol.46, no.12, pp.2553–2559, Dec.1998.

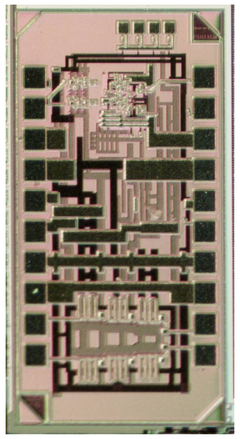
IMPLEMENTATION

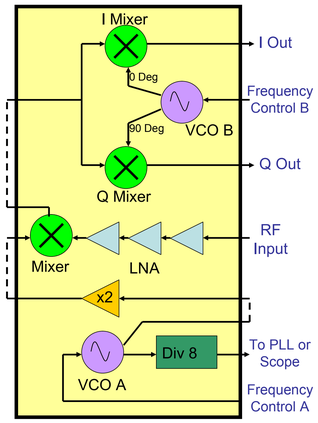


Receiver Chip #1

- •Three cascaded LNA's to achieve 30dB of Gain and desired bandwidth
- •Sampler and Analog Multiplexer to down-convert input signal
- •0.018-0.033THz tunable FFI-VCO compatible with commercial PLL's
- •Complete layout in SiGe and InP

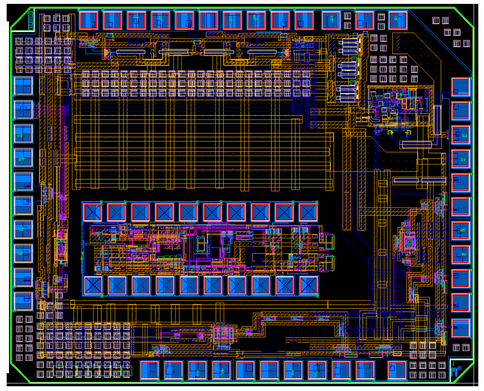




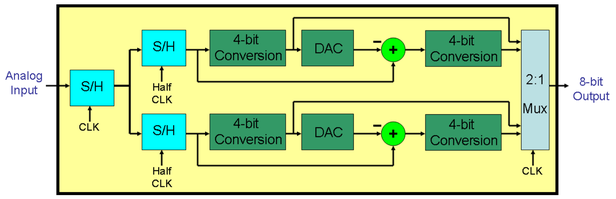


Receiver Chip #2

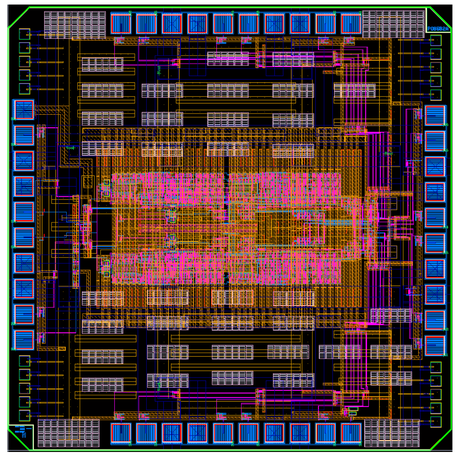
- •Three cascaded LNA's with 30dB of gain to 0.065THz
- •Tunable FFI-VCO with Frequency Doubler to achieve 0.036-0.066THz oscillator
- •Multiple Gilbert mixer down-conversion design
- •Secondary lower speed VCO to perform final signal conversion



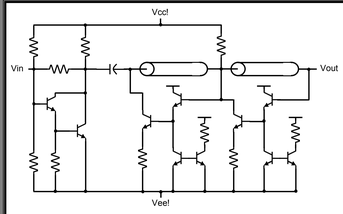
Analog-to-Digital Converter - Test Chip #3



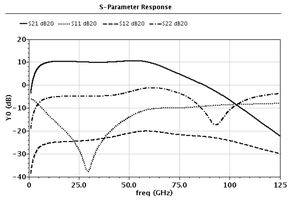
- •Two channel time-interleaved design. Multiplexor stitches the bits from the two channels together to produce the full speed output
- •Full 8-bit conversion completed in two steps. First step generates the Most Significant Bits (MSB's). These are converted back to an analog signal and subtracted from the sampled waveform to produce a residue. This residue is then converted into the Least Significant Bits (LSB's).



SCHEMATICS & DESIGN

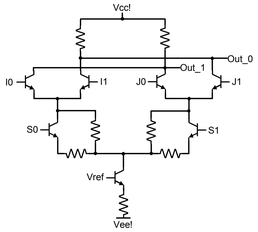


LNA Schematic

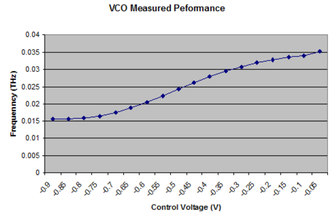


LNA S-Parameter Simulation

Low Noise Amplifier - The most challenging design constraint of the low noise amplifier (LNA) is the large bandwidth sought. To achieve this a matched two-stage approach was taken. The first stage of the LNA is a Darlington pair with resistive feedback. The Darlington pair configuration gives large current gain while the resistive feedback both extends the bandwidth of the amplifier as well as provide impedance matching. The second stage of the LNA consists of cascaded traveling wave amplifiers. Feedback across a transmission line through emitter follower and common emitter configured transistors creates gain at high frequencies in these amplifiers. Timing of signals through the transmission lines and feedback paths in this stage are crucial to achieving gain at a desired frequency. Properly matching this second stage to the first allows for flat gain over a large bandwidth.

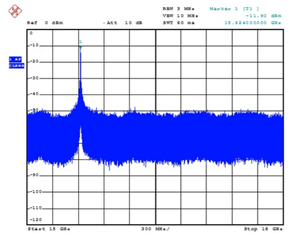


Schematic of Single Stage of VCO

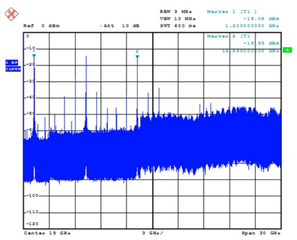


Voltage Controlled Oscillator's Response to Control Voltage (Chip #2)

Voltage Controlled Oscillator – For use in a wideband system a voltage controlled oscillator (VCO) with a large tuning range is desired. To achieve both speed and this tuning capability, a feed forward interpolated VCO was employed. This VCO is a four stage ring oscillator with a 0.019THZ tuning range in SiGe and a 0.035THz tuning range in InP. In simulation the VCO has shown speeds near 0.06THz in InP.



VCO Output Signal at Spectrum Analyzer (Chip #2)



"I" Output Signal with 0.0012 THz Difference between VCO and IF Signals (Chip #2)

FUTURE WORK

Continuing research on circuit topologies and techniques will push for larger bandwidths and increased performance. IBM's current development of 9HP, the next innovation in SiGe BiCMOS technology, will further assist in reaching greater frequencies. Future efforts will primarily focus on analog-to-digital conversion. Exploration of sample-and-hold circuit topologies to allow for high speed and high accuracy conversion is of utmost importance to the project. Building upon the results presented here we look to further push the limits of these circuit technologies

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